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EXAMINER	
DHARIA, PRABODH M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/687,742	KOYAMA, JUN	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-34* is/are pending in the application.

4a) Of the above claim(s) *4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07-20-2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 07-20-2007 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

2. **Status:** Receipt is acknowledged of papers submitted on 07-03-2007 under amendments and new claims, which have been placed of record in the file. Claims 1-3 and 5-34 are pending this action. Claim 4 is cancelled.

Response to Amendment

3. The amendments and new claims filed on 07-03-2007 do not introduce new matter into the disclosure. The added material is supported by the original disclosure.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1,2,7,9,11,12,14-17,19-22, 24-27,29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (US 20030011586 A1) in view of Yanagi et al. (US 2002/0036636 A1).

With respect to **Claim 1**, Nakajima teaches a display device *(See figure 13; [0082])* comprising: a pixel portion *(See figure 13, element 22; See figure 14)* comprising a first thin film transistor *(See figure 14, element 34)* over a substrate and a switching regulator *(See figure 13, element 21: glass substrate; [0083])*; comprising: a switching regulator control circuit *(See figure 13, elements 23U, 25, and 26 comprise a switching regulator control circuit)* comprising a second thin film transistor *(See figure 23: circuit representation of element 26 in figure 13, element Qn12 second thin film transistor; [0095], lines 1-6; [0119], lines 1-5; [0120], lines 1-3)* formed over the substrate *([0092], lines 1-4; note that both the pixel portion and the second thin film transistor are over a substrate).*

However, Nakajima fails to disclose a capacitor electrically connected to the switching element, wherein the switching regulator control circuit is electrically connected to the capacitor for receiving the voltage charged in the capacitor.

However, Yanagi et al. discloses a capacitor electrically connected to the switching element (please see figure 12, page 5, paragraph 70-74), wherein the switching regulator control circuit is electrically connected to the capacitor for receiving the voltage charged in the capacitor (page 5, paragraphs 69-74).

The reason to combine the power supply circuitry of Yanagi specifically helps reduce drop of voltage in different mode of operation at different frequency and different load current, it suppresses interference and power consumption (page 5, paragraph 72,75)

Thus it would have been obvious for a person of ordinary skill in the art at the time the invention was made to have both a pixel portion comprising a first thin film transistor and a switching regulator control circuit comprising a second thin film transistor over a substrate, as

taught by Nakajima, to the display device of Yanagi et al., with switching regulator helps reducing power consumption of the display *(page 5, paragraphs 72,75, page 1, paragraph 6)*.

With respect to **Claim 2**, Nakajima teaches a display device *(See figure 13; [0082])* comprising: a pixel portion *(See figure 13, element 22; See figure 14)* comprising a first thin film transistor *(See figure 14, element 34)* over a substrate and a switching regulator *(See figure 13, element 21: glass ~ substrate; [0083])*; a switching regulator control circuit *(See figure 13, elements 23U, 25, and 26 comprise a switching regulator control circuit)* comprising a second thin film transistor *(See figure 23, element Qp11 ~ second thin film transistor; [0094], lines 11-17)* formed over the substrate *([0092], lines 1-4; note that both the pixel portion and the second thin film transistor are over a substrate)*; wherein a switching element packed on the substrate and *(See figure 23, element Qn1, [0092], lines 1-4; note that both the pixel portion and the second thin film transistor are over a substrate 2)* is driven according to an output signal *(See figure 23, output signal is equivalent to A)* from the switching regulator control circuit to raise or lower the voltage *([0119], note that figure 23 is a charge pump circuit; [0120], note that raising or lowering the voltage is equivalent to a normal mode and a power saving mode)*.

However, Nakajima fails to disclose a capacitor electrically connected to the switching element, wherein the switching regulator control circuit is electrically connected to the capacitor for receiving the voltage charged in the capacitor.

However, Yanagi et al. discloses a capacitor electrically connected to the switching element (please see figure 12, page 5, paragraph 70-74), wherein the switching regulator control

circuit is electrically connected to the capacitor for receiving the voltage charged in the capacitor (page 5, paragraphs 69-74).

The reason to combine the power supply circuitry of Yanagi specifically helps reduce drop of voltage in different mode of operation at different frequency and different load current, it suppresses interference and power consumption (page 5, paragraph 72,75)

Thus it would have been obvious for a person of ordinary skill in the art at the time the invention was made to have both a pixel portion comprising a first thin film transistor and a switching regulator control circuit comprising a second thin film transistor over a substrate, as taught by Nakajima, to the display device of Yanagi et al., with switching regulator helps reducing power consumption of the display *(*page 5, paragraphs 72,75, page 1, paragraph 6*)*.

With respect to **Claim 7**, Nakajima teaches a display device *(See figure 13; [0082])* comprising: a pixel portion *(See figure 13, element 22; See figure 14)* comprising a first thin film transistor *(See figure 14, element 34)* over a substrate *(See figure 13, element 21: glass ~ substrate; [0083])*; and a switching regulator comprising of: a switching regulator control circuit *(See figure 13, elements 23U, 25, and 26 comprise a switching regulator control circuit)* comprising a second thin film transistor *(See figure 23, element Qp11 ~ second thin film transistor; [0094], lines 11-17)* formed over the substrate *([0092], lines 1-4; note that both the pixel portion and the second thin film transistor are over a substrate)*; wherein the switching regulator control circuit uses an analog signal *([0090], lines 6-13; note that the D/A converter converts a digital signal to an analog signal and supplies it to the pixels, thus the switching regulator uses an analog signal).*

However, Nakajima fails to disclose a capacitor electrically connected to the switching element, wherein the switching regulator control circuit is electrically connected to the capacitor for receiving the voltage charged in the capacitor.

However, Yanagi et al. discloses a capacitor electrically connected to the switching element (please see figure 12, page 5, paragraph 70-74), wherein the switching regulator control circuit is electrically connected to the capacitor for receiving the voltage charged in the capacitor (page 5, paragraphs 69-74).

The reason to combine the power supply circuitry of Yanagi specifically helps reduce drop of voltage in different mode of operation at different frequency and different load current, it suppresses interference and power consumption (page 5, paragraph 72,75)

Thus it would have been obvious for a person of ordinary skill in the art at the time the invention was made to have both a pixel portion comprising a first thin film transistor and a switching regulator control circuit comprising a second thin film transistor over a substrate, as taught by Nakajima, to the display device of Yanagi et al., with switching regulator helps reducing power consumption of the display (page 5, paragraphs 72,75, page 1, paragraph 6).

With respect to **Claim 9**, Nakajima teaches a display device *(See figure 13; [0082])* comprising: a pixel portion *(See figure 13, element 22; See figure 14)* comprising a first thin film transistor *(See figure 14, element 34)* over a substrate *(See figure 13, element 21: glass ~ substrate; [0083])*; and a switching regulator control circuit *(See figure 13, elements 23U, 25, and 26 comprise a switching regulator control circuit)* comprising a second thin film transistor

(See figure 23: circuit representation of element 26 in figure 13, element Qn12 ~ second thin film transistor; [0095], lines 1-6; [0119], lines 1-5; [0120], lines 1-3) over the substrate *([0092], lines 1-4; note that both the pixel portion and the second thin film transistor are over a substrate)*, wherein the switching regulator control circuit uses a digital signal *(See figure 15, element 44U, please note the D/A converter within the switching regulator control circuit)*.

However, Nakajima fails to disclose a capacitor electrically connected to the switching element, wherein the switching regulator control circuit is electrically connected to the capacitor for receiving the voltage charged in the capacitor.

However, Yanagi et al. discloses a capacitor electrically connected to the switching element (please see figure 12, page 5, paragraph 70-74), wherein the switching regulator control circuit is electrically connected to the capacitor for receiving the voltage charged in the capacitor (page 5, paragraphs 69-74).

The reason to combine the power supply circuitry of Yanagi specifically helps reduce drop of voltage in different mode of operation at different frequency and different load current, it suppresses interference and power consumption (page 5, paragraph 72,75)

Thus it would have been obvious for a person of ordinary skill in the art at the time the invention was made to have both a pixel portion comprising a first thin film transistor and a switching regulator control circuit comprising a second thin film transistor over a substrate, as taught by Nakajima, to the display device of Yanagi et al., with switching regulator helps reducing power consumption of the display *(page 5, paragraphs 72,75, page 1, paragraph 6)*.

With respect to **Claims 11, 12, and 14-15**, a display device according to claims 1, 2, 7 and 9 respectively, Nakajima teaches a plurality of switching regulator control circuits are formed over the substrate *(See figure 13, elements 23U, 25, and 26: 1st switching regulator control circuit, elements 23D, 25, and 26: 2nd switching regulator control circuit, elements 24, 25, and 26: 3rd switching regulator control circuits).*

With respect to **Claims 16, 17 and 19-20**, a display device according to claims 1, 2, 7 and 9 respectively, Nakajima teaches the display device is a liquid crystal display device *([0081]).*

With respect to **Claims 21, 22 and 24-25**, a display device according to claims 1, 2, 7 and 9 respectively, Nakajima teaches the display device is an EL display device *([0181]).*

With respect to **Claims 26, 27 and 29-30**, a display device according to claim 1, 2, 7 and 9 respectively, Nakajima teaches the display device is applied to electronic equipment selected form a group consisting of personal computers, a display unit of portable terminals such as portable telephones, and PDAs *([0182]).*

5. **Claims 31-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (US 20030011586 A1) in view of Yanagi et al. (US 2002/0036636 A1) as applied to Claims 1,2,7,9,11,12,14-17,19-22, 24-27,29 and 30 above, and further in view of Ishiyama (US 20050052447 A1).

Regarding **Claims 31,33 and 34** Nakajima fails to disclose a switching element packed on a FPC, and driven according to an output signal from said switching regulator control circuit to raise or lower a voltage and wherein the switching regulator control circuit uses a digital signal

However, Ishiyama discloses a switching element packed on a FPC (page 14, paragraph 297, FPC substrate with element 40, page 2, paragraph 43 a switching regulator or booster circuit figure 1, element 40), and driven according to an output signal from said switching regulator control circuit to raise or lower a voltage (pages 11, paragraphs 252-254 see figures 11-13) and wherein the switching regulator control circuit uses a digital signal (pages 11,12, paragraphs 258-267).

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have both a pixel portion comprising a first thin film transistor and a switching regulator control circuit comprising a second thin film transistor over a substrate, as taught by Nakajima, to the display device of Ishiyama, with switching regulator helps reducing power consumption of the display *(page 1, paragraphs 2,3)*.

6. **Claims 3, 6, 18, 23 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai et al. (Pub. No.: US 2002/0175662 A1) in view of Nakajima (US 20030011586 A1) and Sato et al. (US 5,583,424).

With respect to **Claim 3**, Sakurai teaches a display device comprising *(See figure 5 and figure 3 where figure 3 is equivalent to element 100)*: a pixel portion comprising a first thin film

transistor *(See figure 5, element 180; [0007], lines 3-6; [0069], lines 9-13)*; and a switching regulator comprising of: a switching regulator control circuit *(See figure 3, switching regulator control circuit ~ element 34 and 70)* comprising a second transistor *(element Q1)*; a switching element *(element Q2)*; an inductor *(L1)*; a diode *(D1)*; and a smoothing capacitor *(C2)*, wherein the switching regulator control circuit comprises: a voltage feed back circuit which feeds back a voltage of the smoothing capacitor *([0035])*; and a duty control circuit which controls a switching duty of the switching element *(See figure 3, duty control circuit ~ DC/DC converter control circuit)*.

Although Sakurai uses a transistor, it would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a thin film transistor as the second transistor in the switching regulator control circuit of Sakurai so as to provide higher reliability and faster response time as characteristic of a thin film transistor.

Sakurai does not mention a pixel portion and a second thin film transistor both over a substrate.

Nakajima teaches a pixel portion *(See figure 13, element 22; See figure 14)* comprising a first thin film transistor *(See figure 14, element 34)* over a substrate *(See figure 13, element 21: glass ~ substrate; [0083])*; a switching regulator control circuit *(See figure 13, elements 23U, 25, and 26 comprise a switching regulator control circuit)* comprising a second thin film transistor *(See figure 23, element Qp11 ~ second thin film transistor)* over the substrate *([0092], lines 1-4; note that both the pixel portion and the second thin film transistor are over a substrate)*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have both a pixel portion comprising a first thin film transistor and a

switching regulator control circuit comprising a second thin film transistor over a substrate, as taught by Nakajima, to the display device of Sakurai, so as to produce circuits that are manufactured more easily and realized at a lower cost *([0094], lines 12-20)*.

Sakurai, fails to disclose a smoothing capacitor electrically connected to the switching element, wherein said switching regulator control circuit comprises: a voltage feed back circuit electrically connected to the smoothing capacitor for receiving a voltage charged in the smoothing capacitor; and a duty control circuit which controls a switching duty of said switching element.

However, Sato et al. discloses a smoothing capacitor electrically connected to the switching element (please see figure 9A-9E, 16, 17 and 36, Col. 16, Lines 28-51, Col. 10, Lines 9-32), wherein said switching regulator control circuit comprises: a voltage feed back circuit electrically connected to the smoothing capacitor for receiving a voltage charged in the smoothing capacitor (Col. 2, Line 57 to Col. 3, Line 23 please see figure 9A-9E, 16, 17 and 36, Col. 16, Lines 28-51, Col. 10, Lines 9-32); and a duty control circuit which controls a switching duty of said switching element (Col. 2, Line 57 to Col. 3, Line 23 please see figure 9A-9E, 16, 17 and 36, Col. 16, Lines 28-51, Col. 10, Lines 9-32).

The reason to combine the voltage supplying smoothing capacitor using proper feed back circuitry maintained at constant voltage and reduce loss due to over current. Also in the display application the high voltage pulses are smoothed with diode and smoothing capacitor. The overall power supply is simplified and made compact for a flat Panel display.

Thus it would have been obvious for a person of ordinary skill in the art at the time the invention was made to have both a pixel portion comprising a first thin film transistor and a

switching regulator control circuit comprising a second thin film transistor over a substrate, as taught by Sakurai, to the display device and compact power supply of Sato et al., with switching regulator helps reducing power consumption of the display, reduces current loss and smoothens the high voltage driving pulses *(Col. 1, Lines 6-10, Col. 2, Lines 33-39,Col. 23, Lines 27-30,Col. 24, lines 3-8)*.

With respect to **Claim 6**, a display device according to claim 3, Sakurai teaches the switching element is made up of a transistor *(See figure 3, switching element ~ Q2)*.

Although Sakurai uses a transistor, it would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a thin film transistor as the switching element in the display device of Sakurai so as to provide higher reliability and faster response time as characteristic of a thin film transistor.

With respect to **Claim 18**, a display device according to claim 3, Sakurai teaches the display device is a liquid crystal display device *([0066])*.

With respect to **Claim 23**, a display device according to claim 3, Sakurai does not mention the display device is an EL display device.

Nakajima teaches the display device is an EL display device *([0181])*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a display device that is an EL display device, as taught by Nakajima to the display device of Sakurai, so as to have a greater range of applicability.

With respect to **Claim 28**, a display device according to claim 3, Sakurai does not mention the display device is applied to electronic equipment selected from a group consisting of a digital camera, a notebook type personal computer, a PDA, a DVD player, a folding portable display device, a watch type display device and a mobile telephone.

Nakajima teaches the display device is applied to electronic equipment selected form a group consisting of personal computers, a display unit of portable terminals such as portable telephones, and PDAs *([0182])*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a display device applied to electronic equipment selected from a group consisting of personal computers, a display unit of portable terminals such as portable telephones, and PDAs, as taught by Nakajima, to the display device of Sakurai, so as to have a greater range of applicability.

7. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai (Pub. No.: US 2002/0175662 A1); Nakajima (US 20030011586 A1) and Sato et al. (US 5,583,424) as applied to claim 3 above, and further in view of Ayres (Pub. No.: US 2001/0007432 A1).

With respect to **Claim 5**, a display device according to claim 3, Sakurai, Nakajima and Sato et al. do not teach a display device wherein the inductor, the diode, and the smoothing capacitor are packed on a substrate. However, Nakajima teaches an inductor is used in a conventional liquid crystal display apparatus *([0004])* and is not required for a charge pump DD converter.

Nakajima and Sato et al. modifies the display device of Sakurai such that the inductor is packed on the substrate since the inductor is part of the switching regulator control circuit.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use an inductor packed on a substrate, as taught by Nakajima modified by Sato et al., to the display device of Sakurai, so as to further enhance the operability of the display device in exchange for size *([0004])*.

Ayres teaches an active matrix liquid crystal display *([0001], lines 4-8)* where a diode *(See figure 10, element 10; [0028])* and a capacitor *(See figure 1, element 12; [0021])* are packed on the same substrate as a pixel portion *([0015])*.

Ayres modifies the display device of Sakurai as modified by Nakajima and Sato et al. such that the diode is a pin diode.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to pack a diode and a smoothing capacitor on a substrate as taught by Ayres, to the display device of Sakurai as modified by Nakajima modified by Sato et al., so as to enable the circuit to be formed on the same thin-film processing as may be required for other elements of the circuit *([0007])* in effect reducing costs and easing manufacturing.

8. **Claim 32** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai (Pub. No.: US 2002/0175662 A1); Nakajima (US 20030011586 A1) and Sato et al. (US 5,583,424) as applied to claim 3 above, and further in view of Ishiyama (US 20050052447 A1).

Regarding **Claim 32** Sakurai modified by Nakajima and Sato et al. fails to disclose a switching element packed on a FPC, and driven according to an output signal from said switching regulator control circuit to raise or lower a voltage and wherein the switching regulator control circuit uses a digital signal

However, Ishiyama discloses a switching element packed on a FPC (page 14, paragraph 297, FPC substrate with element 40, page 2, paragraph 43 a switching regulator or booster circuit figure 1, element 40), and driven according to an output signal from said switching regulator control circuit to raise or lower a voltage (pages 11, paragraphs 252-254 see figures 11-13) and wherein the switching regulator control circuit uses a digital signal (pages 11,12, paragraphs 258-267).

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have both a pixel portion comprising a first thin film transistor and a switching regulator control circuit comprising a second thin film transistor over a substrate, as taught by Sakurai modified by Nakajima and Sato et al, to the display device of Ishiyama, with switching regulator helps reducing power consumption of the display *(page 1, paragraphs 2,3)*.

9. **Claims 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (US 20030011586 A1) and Yanagi et al. (US 2002/0036636 A1) as applied to claim 9 above, and further in view of Tomio et al. (Pub. No.: US 2002/0044145 A1).

With respect to **Claim 10**, as per Claim 9 above Nakajima (US 20030011586 A1) and Yanagi et al. (US 2002/0036636 A1) fails to teach the switching regulator control circuit comprises an AD converter circuit, a frame memory, a CPU and a pulse generation circuit.

However, Tomio discloses a display device *(See figure 5)* comprising: a pixel portion *(See figure 5, element 30)* over a substrate *([0041]; the substrate is equivalent to glass)*; and a switching regulator control circuit *(elements 40 and 50)* comprising a transistor, wherein the switching regulator control circuit uses an analog signal a display device according to claim 9,

Tomio teaches the switching regulator control circuit comprises an AD converter circuit *(See figure 6A, A/D)*, a frame memory *(See figure 5, element 12)*, a CPU *(See figure 5, element 40; [0077], lines 1-6)*, and a pulse generation circuit *(element 21 and 23; [0050])*.a display device *(See figure 5)* comprising: a pixel portion *(See figure 5, element 30)* over a substrate *([0041]; the substrate is equivalent to glass)*; and a switching regulator control circuit *(elements 40 and 50)* comprising a transistor, wherein the switching regulator control circuit uses an analog signal *([0077], lines 1-3; analog signals ~ VAK, VWK, VEK, VSK)*. Tomio teaches the display device can be employed in a liquid crystal display but does not mention a pixel portion comprising a first thin film transistor over a substrate nor does Tomio mention a second thin film transistor over a substrate.

Although Tomio uses a transistor *(figure 8: element 50; Tr71 – Tr73)*, it would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a thin film transistor in the switching regulator control circuit of Tomio so as to provide higher reliability and faster response time as characteristic of a thin film transistor.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a pixel portion comprised of a first thin film transistor over a substrate and a second thin film transistor over a substrate, as taught by Nakajima modified by Yanagi et al., to the display device of Tomio, so as to obtain a high current capacity on a small-area circuit scale ([0020]) and to produce circuits that are manufactured more easily and realized at a lower cost *([0094], lines 12-20)*.

10. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (US 20030011586 A1) and Yanagi et al. (US 2002/0036636 A1) as applied to claim 7 above, and further in view of Yu (Pub. No.: Us 2003/0201967 A1).

With respect to **Claim 8**, Nakajima and Yanagi et al. fails to disclose a switching regulator control circuit comprising a reference voltage source, a triangle wave generation circuit, an error amplification circuit and a PWM comparator.

Yu teaches a switching regulator control circuit comprising a reference voltage source *(figure 3, Vref; [0033], last two lines)*, a triangle wave generation circuit *(figure 3, element 336; [0030], lines 1-2)*, an error amplification circuit *(figure 3, element 303; [0033], last three lines)* and a PWM comparator *(figure 3, element 302; [0033], last three lines)*.

Yu modifies the display device of Nakajima and Yanagi et al., by replacing the switching regulator control circuit with that of Yu (control integrated circuit) as shown in figure 3 since the control integrated circuit provides the same function for stabilization of current, while maintain the transistors as thin film transistors.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to use a switching regulator circuit, as taught by Yu to the display device modified by Nakajima and Yanagi et al. so as to provide stabilization of current *([0010])*.

11. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai (Pub. No.: US 2002/0175662 A1); Nakajima (US 20030011586 A1) and Sato et al. (US 5,583,424) as applied to claim 3 above, and further in view of Muthu et al. (Pub. No.: US 2002/0145041).

With respect to **Claim 13**, a display device according to claim 3, Sakurai and Nakajima do not teach a plurality of switching regulator control circuits are formed over the substrate.

Muthu teaches an LED based freezer driver *(See figure 1; [0016])* in which a plurality *(See figure 1, elements 30, 31, and 32)* of switching regulator control circuits are formed for each of red, green, and blue lights *([0005], lines 6-10)*. Although Muthu teaches an LED driver, Muthu mentions that LED illumination is applicable in backlighting for LCD panels *([0002], lines 1-3)* as does Sakurai teaches vice versa is true of an LCD panel *([0099])*.

Muthu modifies the display device of Sakurai as modified by Nakajima and Sato et al. such that a plurality of switching regulator control circuits are formed over the

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to modify the display device of Sakurai as modified by Nakajima and Sato et al., to have a plurality of switching regulator control circuits, as taught by Muthu, resulting in a plurality of switching regulator control circuits over a substrate so as to adjust values of each of

the red, green, and blue lights to achieve prescribed lighting intensity and color *([0005], lines 6-10)*.

Response to Arguments

12. Applicant's arguments with respect to amended independent claims 1,2,3,7 and 9 and new claim 31-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

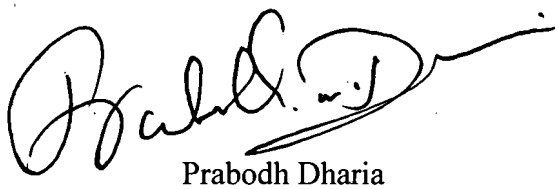
15. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231



Prabodh Dharia

Full Signatory Authority Program

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